CONTINUOUS INTERNAL EVALUATION- 1

Dept:ECE	Sem / Div:5 ECE	Sub:Verilog HDL	S Code:18EC56
Date:21-10-2020	Time:2:30 -4:00PM	Max Marks: 50	Elective:N

Note: Answer any 2 full questions, choosing one full question from each part.

QN	Questions	Marks	RBT	COs
	PART A			
1 a	Explain the typical design flow for designing VLSI IC circuits,with a neat flowchart.	8	L2	CO1
b	Declare the following variables in verilog a. An 8-bit vector net called *a_in*. b. A 32-bit storage register called address. Bit 31 must be the most significant bit. Set the value of the register to a 32-bit decimal number equal to 3. c. An array called delays. Array contains 20 elements of the type integer. d. A memory MEM containing 256 words of 64 bits each.	5	L3	CO2
c	Explain the importance and popularity of Verilog HDL	6	L2	CO1
d	What are the basic components of a module? Explain all the components of a module with a neat block diagram.	6	L2	CO2
	OR			
2 a	Write verilog description of SR Latch using instantiation. Also write stimulus code.	9	L3	CO2
b	Explain the top-down design methodology. Explain instantiation. Consider the example of 4 bit ripple carry counter write the verilog description for design block and also for stimulus block.	10	L3	CO1
c	Explain system tasks and compiler directives in verilog.	6	L2	CO2
	PART B			
3 a	Explain the trends in Hardware description Languages (HDLs)	6	L2	CO1
b	Explain module and module instances.	6	L2	CO1
c	Explain the port connection rules	5	L2	CO2
d	Explain the following data types with an example in verilog:(i) Nets (ii) Register (iii) integers (iv) Real (v) Time Register	8	L2	CO2
	OR			
4 a	Explain the two methods of connecting ports to external signals with an example(4 bit adder)	9	L2	CO2
b	Explain the different levels of abstraction used for programming in verilog.	6	L2	CO1
c	Explain the two steps of stimulus application	5	L2	CO1
d	For a 4-bit parallel shift register shown in the figure (i) Write the module definition. Include the list of ports and port declarations. (do not need to show the internals.) (ii) Declare a top-level module stimulus. Define REG_IN (4 bit) and CLK (1 bit) as reg register variables and REG_OUT (4 bit) as wire. Instantiate the module shift_reg and call it sr1. Connect the ports by ordered list.	5	L3	CO2

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HOD

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