## Vivekananda College of Engineering & Technology, Puttur [A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®]

Affiliated to VTU, Belagavi & Approved by AICTE New Delhi

CRM08

Rev 1.10

19-10-2020

## CONTINUOUS INTERNAL EVALUATION- 1

Dept:ECE

Sem / Div:5 ECE

Sub:Verilog HDL

S Code:18EC56

Date:21-10-2020

Time:2:30 -4:00PM

Max Marks: 50

Elective:N

Note: Answer any 2 full questions, choosing one full question from each part.

	8	L2	programme (
	(00	L2	ping ping raw
	5		COI
decimal number ents of the type	2	L3	CO2
.011.	6	1.0	CO1
Explain all the	E - 1	L2	CO2
ution. Also write	9	L3	CO2
vrite the verilog	0	L3	CO1
g. (	5	L2	CO2
(HDLs)	5	L2	CO1
(	5	L2	CO1
5	5	L.2	CO2
verilog:(i) Nets 8	3	L2	CO2
		L2	CO2
orogramming in 6		L2	COI
5		10	CO1
ports and port  _IN (4 bit) and		L3	CO2
	Explain all the ation. Also write  Write the verilog ck.  g.  (HDLs)  verilog:(i) Nets  standard signals with  programming in  6	ents of the type  ach.  Explain all the 6  ation. Also write 9  10  write the verilog ek.  g. 6  s (HDLs) 6  verilog:(i) Nets 8  nal signals with 9  programming in 6  programming in 6  10  10  10  10  10  10  10  10  10  1	ents of the type  ach.  Explain all the 6 L2  ation. Also write 9 L3  10 L3  write the verilog ek.  g. 6 L2  s (HDLs) 6 L2  s (HDLs) 6 L2  verilog:(i) Nets 8 L2  nal signals with 9 L2  programming in 6 L2  programming in 6 L2  s L2  s L2  s L3  ports and port  IN (4 bit) and  a L4  IN (4 bit) and  a L5  IN (4 bit) and  a L5  IN (4 bit) and

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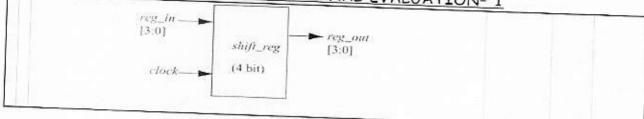
ECE

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Prepared by: Jovita Lasrado

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